

FIGURE 1A

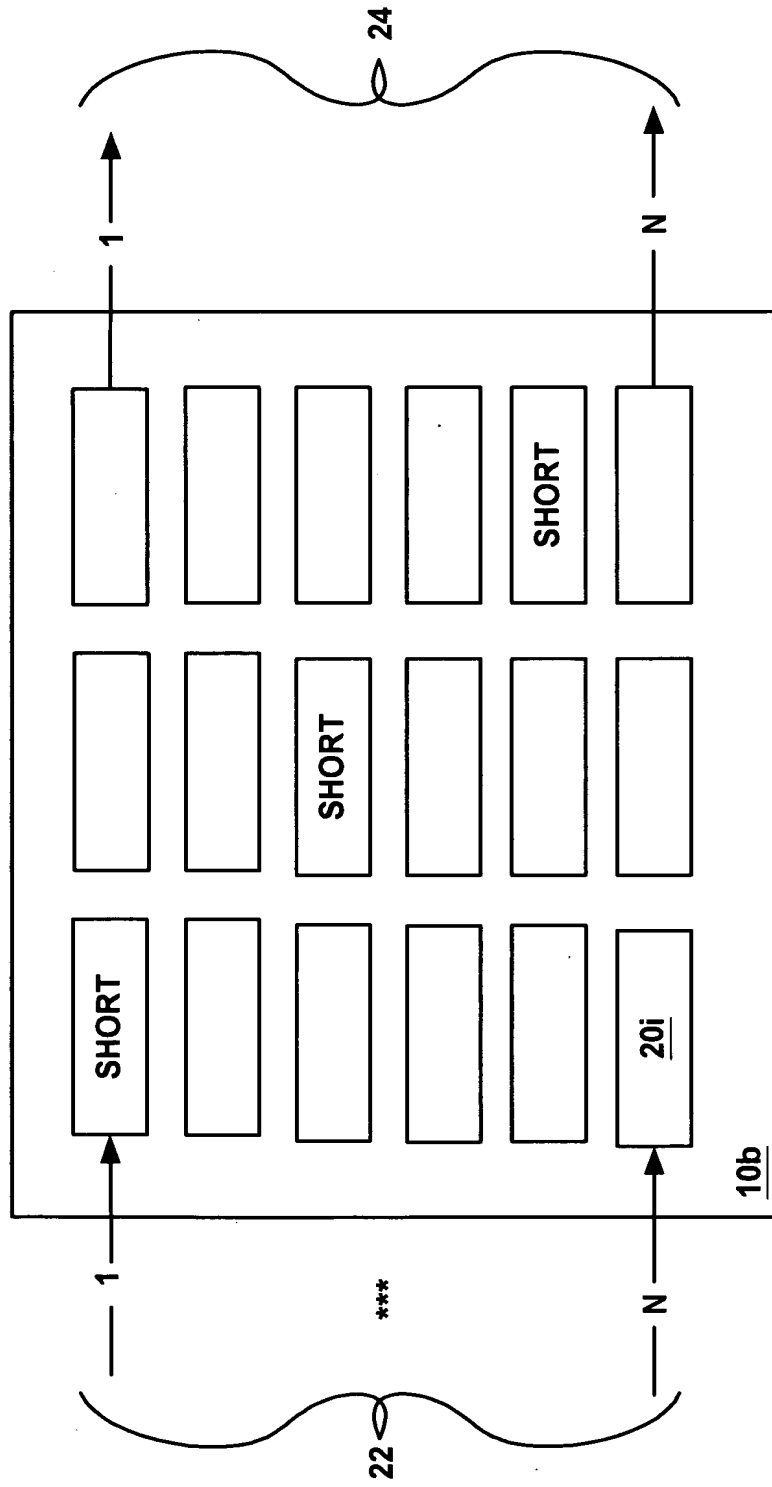


FIGURE 1B

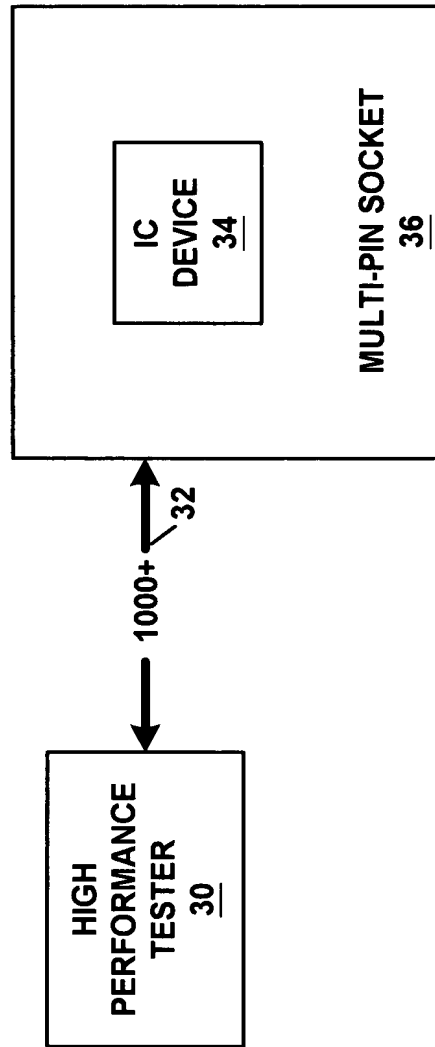


FIGURE 1C

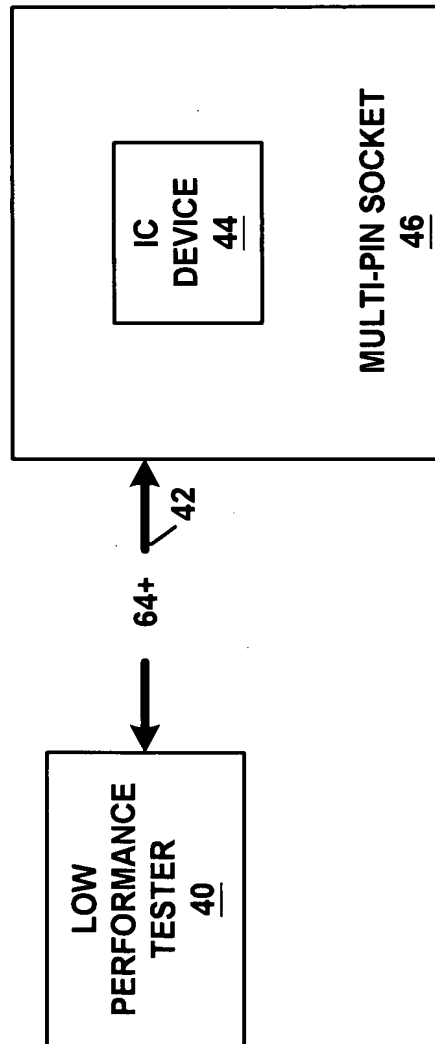
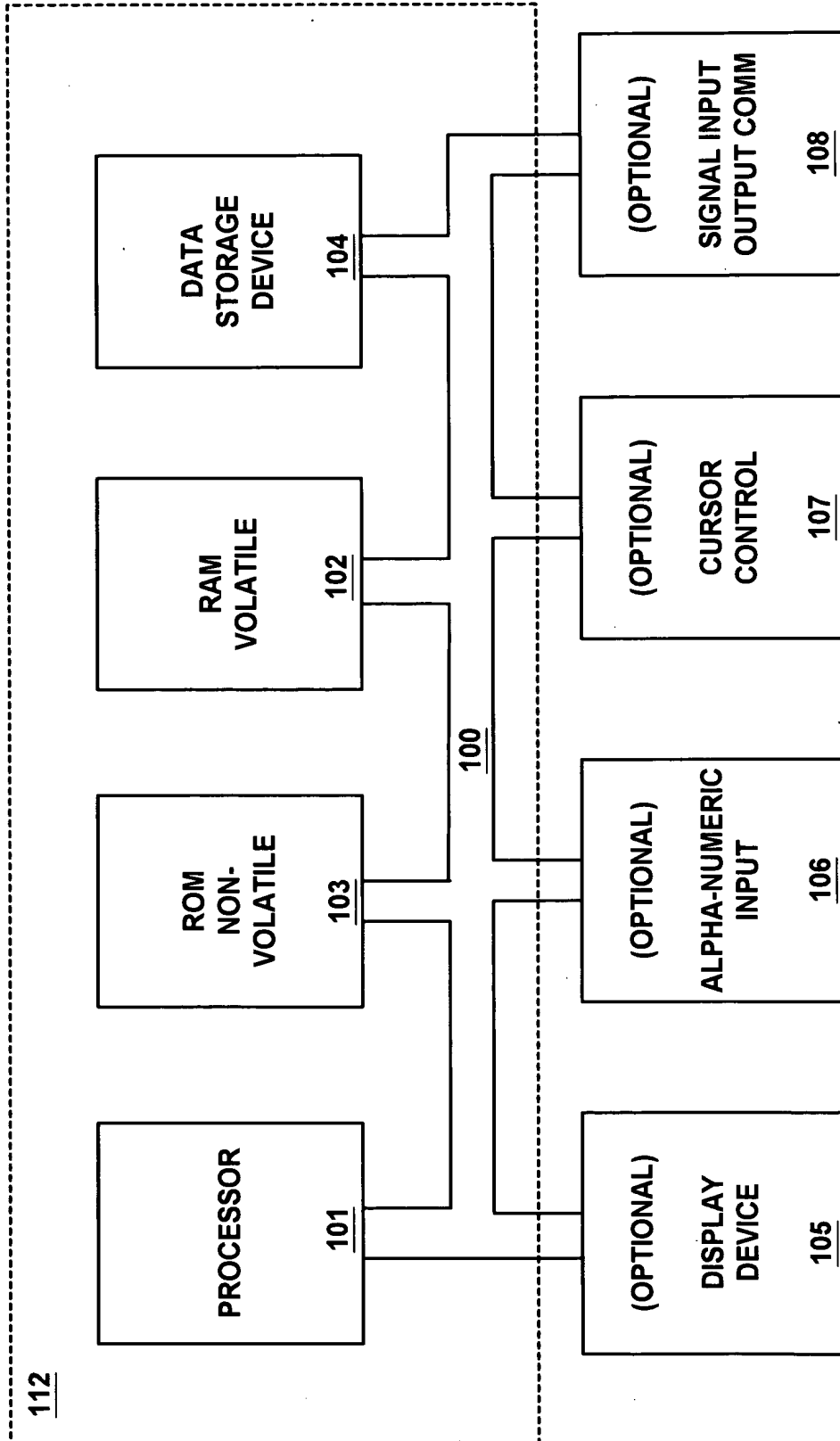
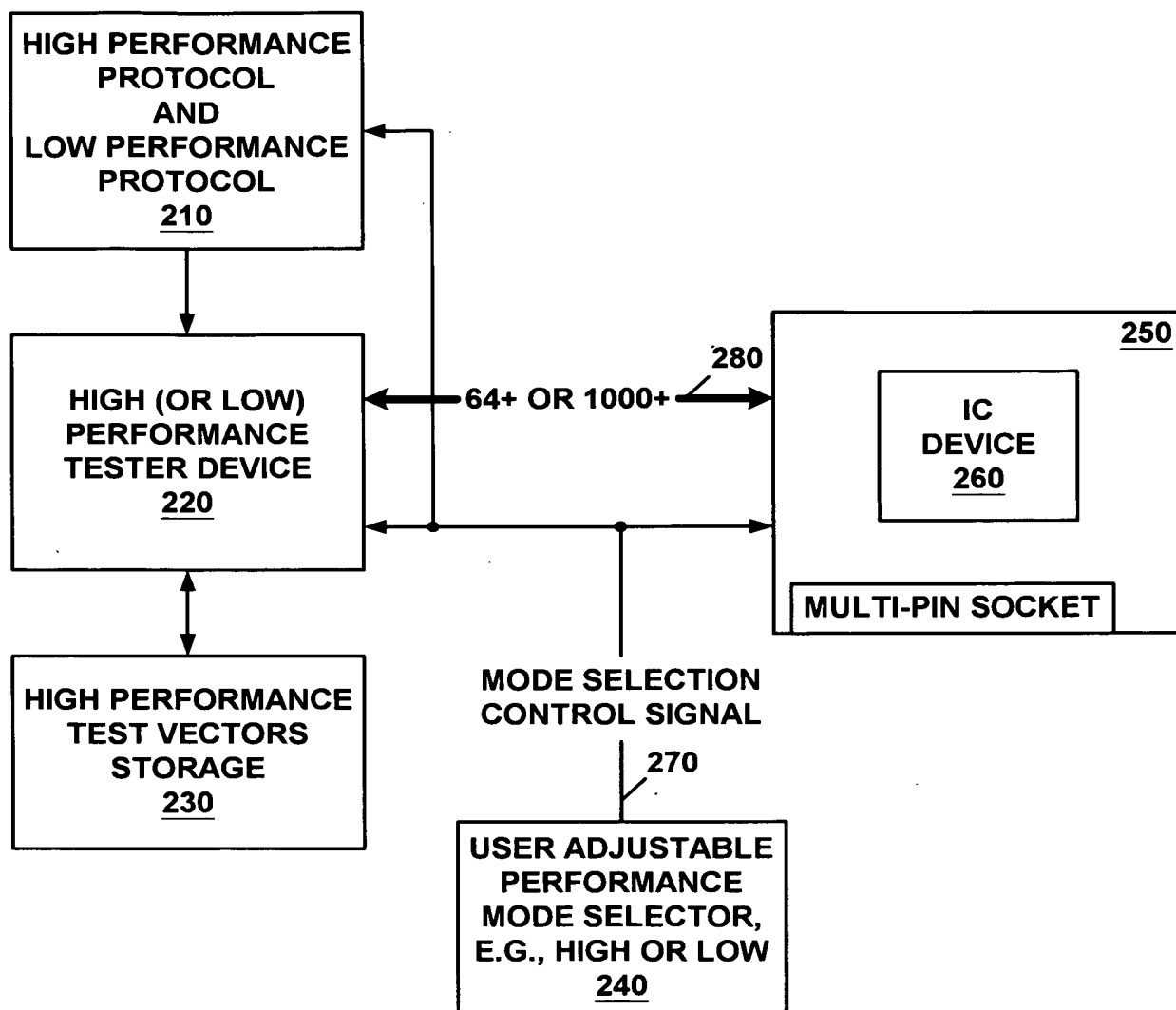


FIGURE 1D

**FIGURE 2**

**FIGURE 3**

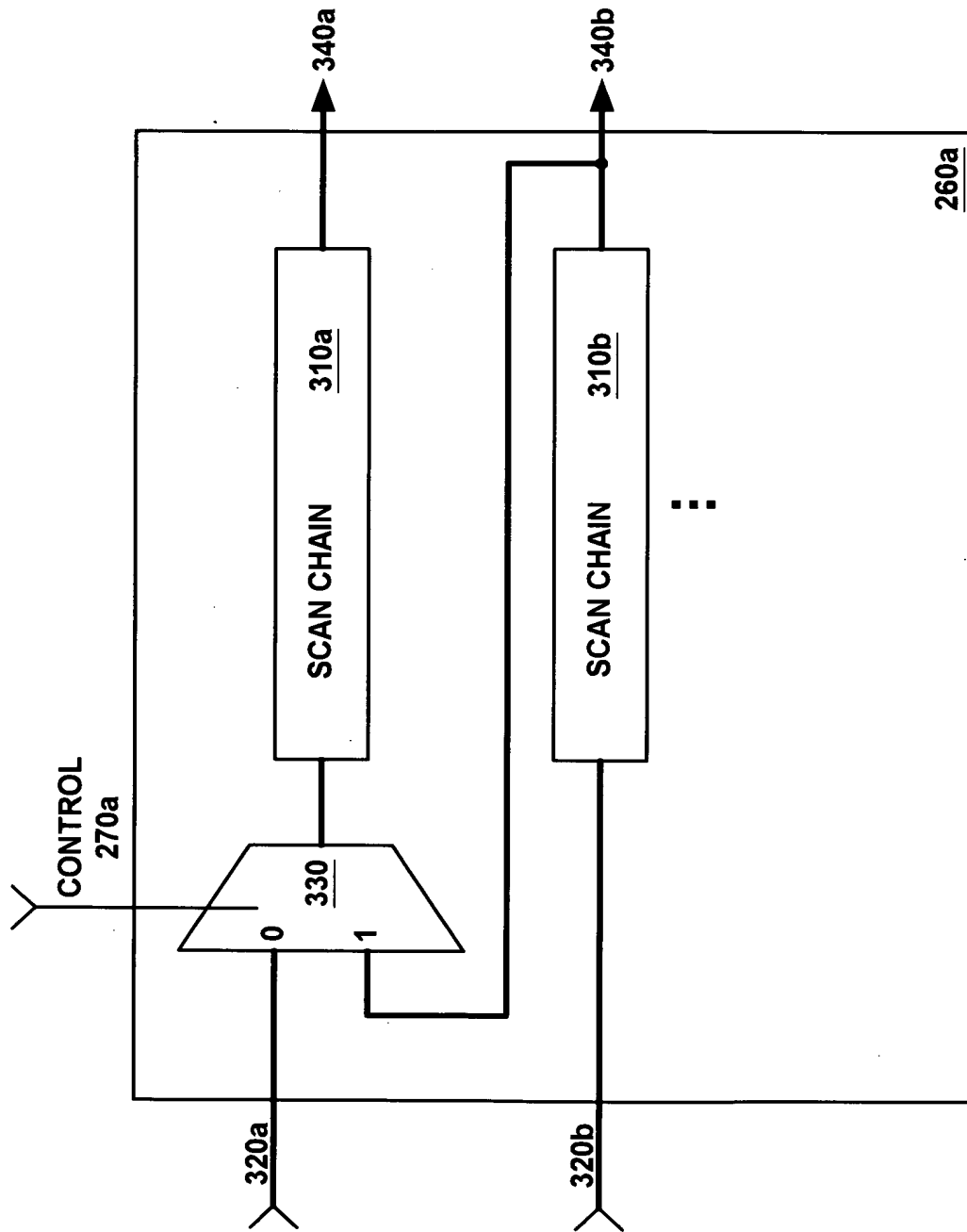
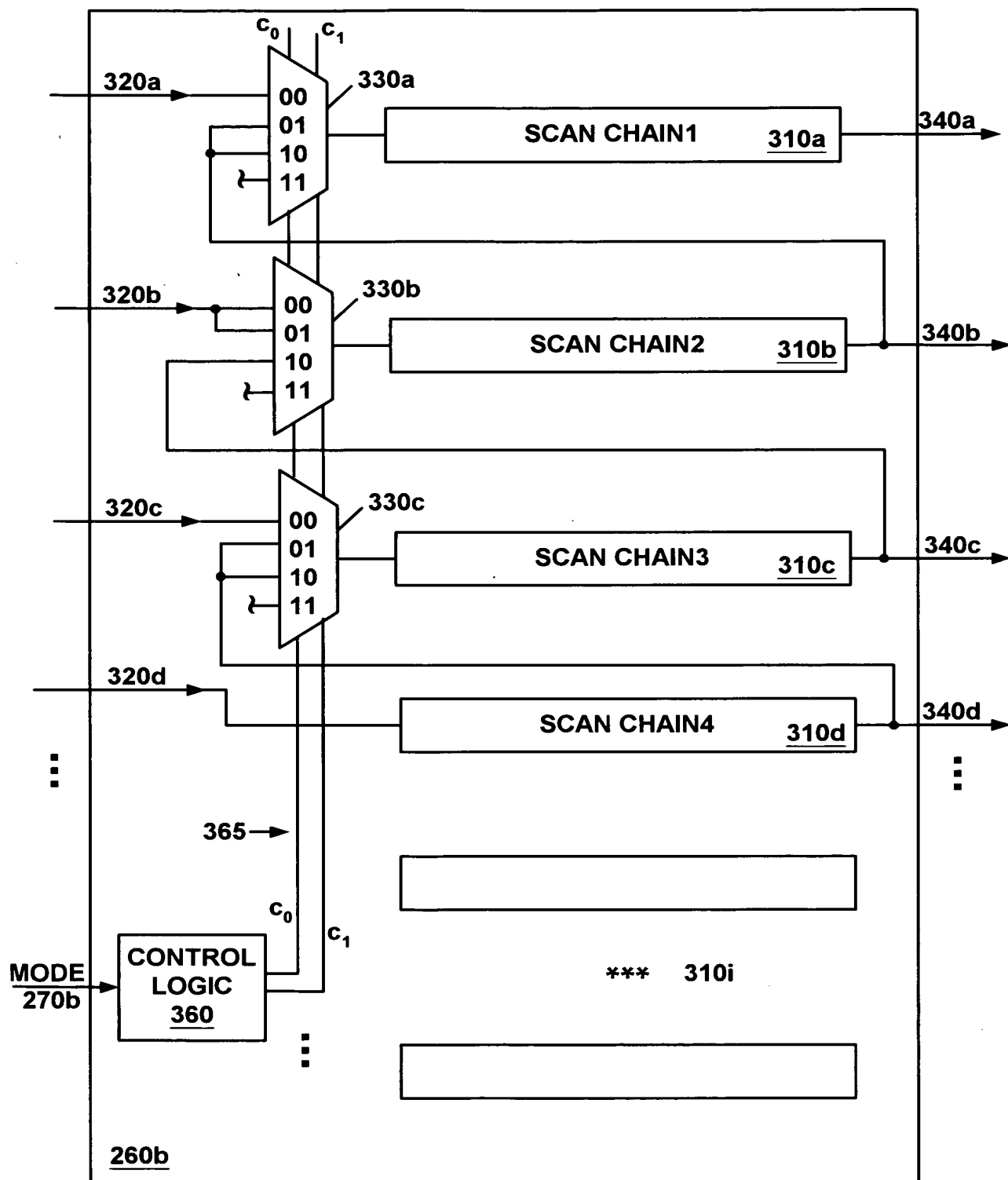
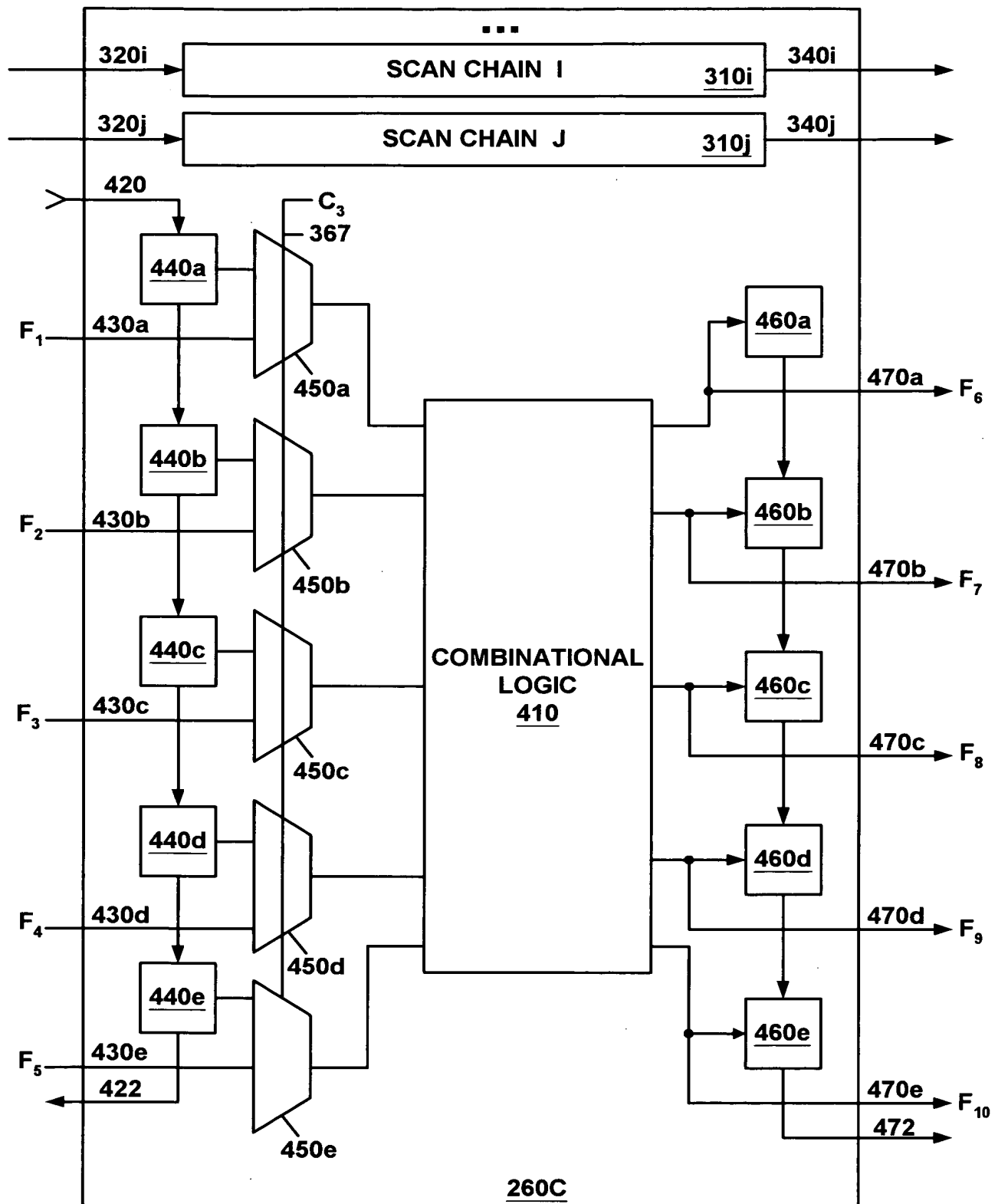
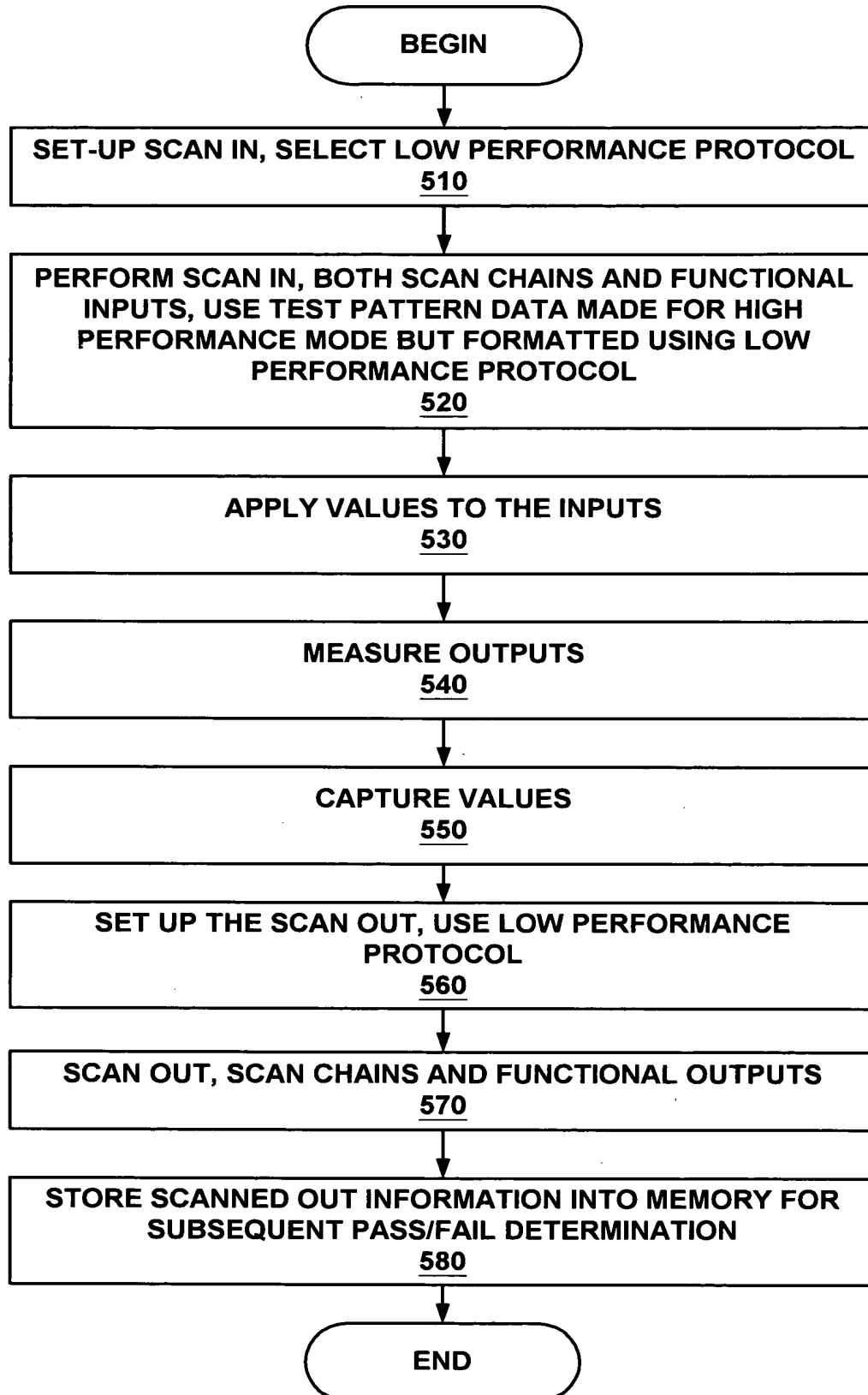


FIGURE 4A

**FIGURE 4B**

**FIGURE 5**

**FIGURE 6**

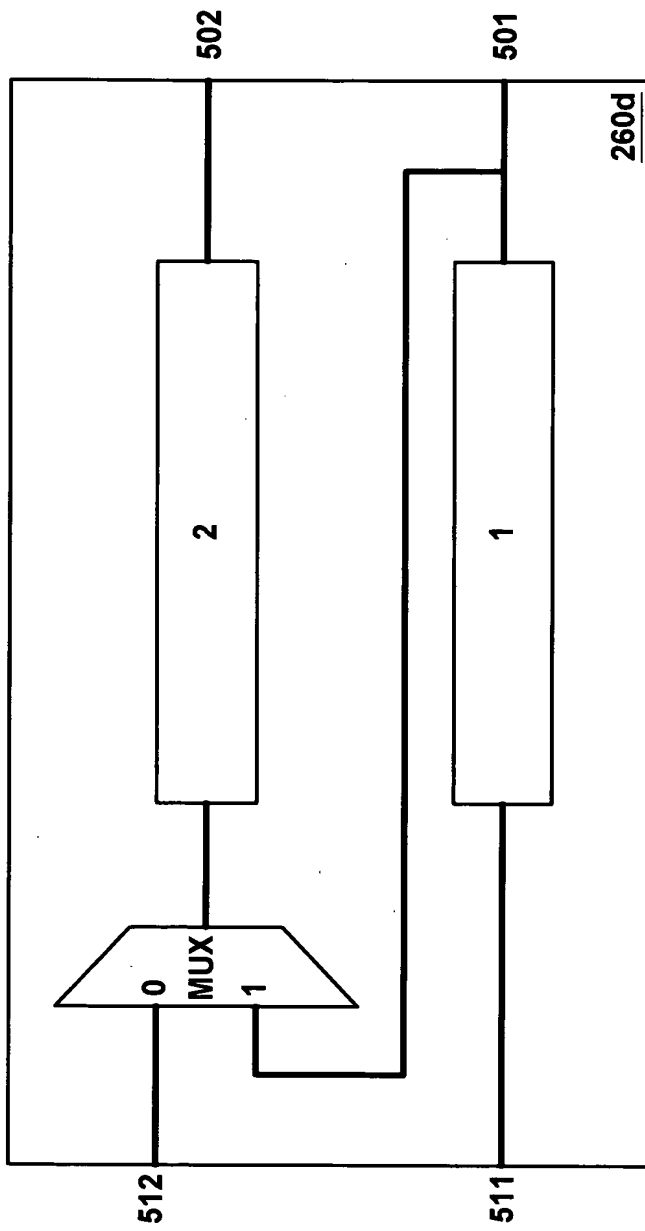


FIGURE 7A

```

MacroDefs {
  Do_one_test {
    W normal_timing;
    C { scan_enable = 1; control_inputs = 'control_inputs'; }
    If ( reconfig_signal == many_inputs )
    {
      640 → Shift { V { si1 = 'si1'; si2 = 'si2'; so1 = 'S01_p'; so2 = 'S02_p'; clk' = P; }}
      C { scan_enable = 0; }
      V { func_inputs = 'func_inputs'; func_outputs = 'func_outputs'; } ← 650
    }
    If ( reconfig_signal == few_inputs )
    {
      Shift { V { si1 = 'si1 si2'; so2 = 'so2 so1'; ← 660
        funcIn = 'func_inputs'; funcOut = 'func_outputs_p'clk = P; } ← 670
      C { scan_enable = 0; }
    }
    V { clk = P; } — 680
  }
}

```

FIGURE 7B